Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-3. (cancelled).

4. (currently amended) A digital filter having a plurality of digital filter elements which are connected to each other in series, each digital filter element comprising:

at least one forward coefficient multiplication circuit;

at least one backward coefficient multiplication circuit;

an adder logic circuit which performs an addition operation of an input signal and ~~the~~ an output signal of said backward coefficient multiplication circuit;

a storage circuit which serves to store ~~the~~ an output signal of said adder logic circuit;

an overflow detecting circuit which receives the output signal of said backward coefficient multiplication circuit, ~~the~~ an output signal of the forward coefficient multiplication circuit in the preceding stage and all of the carry signals to the MSB(most significant bit)s from ~~the~~ adjacent lower bits in summation of the output signals of said backward and forward coefficient multiplication circuits in the current and preceding stages respectively and which serves to detect an overflow occurring in the output signal of said adder logic circuit; and

a clipping circuit connected to said storage circuit in order to clip ~~the~~ an output signal of said storage circuit to either a positive or negative predetermined fixed value and output the clipped value in accordance with ~~the~~ an output signal of said overflow detecting circuit.

5. (currently amended) A digital filter having a plurality of digital filter elements which are connected to each other in series, each digital filter element comprising:

at least one forward coefficient multiplication circuit;

at least one backward coefficient multiplication circuit;

an adder logic circuit which performs an addition operation of an input signal and ~~the~~ an output signal of said backward coefficient multiplication circuit;

a first storage circuit which serves to store the output signal of said adder logic circuit;

an overflow detecting circuit which receives the output signal of said backward coefficient multiplication circuit, ~~the~~ an output signal of the forward coefficient multiplication circuit in the preceding stage, all of the carry signals to the MSB(most significant bit)s from ~~the~~ adjacent lower bits in summation of the output signals of said backward and forward coefficient multiplication circuits in the current and preceding stages respectively and the input and output signals of said first storage circuit and which serves to detect an overflow occurring in the output signal of said adder logic circuit;

a second storage circuit which stores the output signal of said first storage circuit; and

a clipping circuit connected to said second storage circuit in order to clip ~~the~~ an output signal of said second storage circuit to either a positive or negative predetermined fixed value and output the clipped value in accordance with ~~the~~ an output signal of said overflow detecting circuit.

6. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

a logical inversion circuit which serves to perform logical inversion of said output signals of the backward and forward coefficient multiplication circuits;

an adder logic circuit which serves to sum up ~~the~~ an output signal of said logical inversion circuit and said carry signals; and

a decoding circuit which serves to decode ~~the~~ an output signal of said adder logic circuit.

7. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

a logical inversion circuit which serves to perform logical inversion of said output signals of the backward and forward coefficient multiplication circuits;

an adder logic circuit which serves to sum up ~~the~~ an output signal of said logical inversion circuit and said carry signals; and

a decoding circuit which serves to decode ~~the~~ an output signal of said adder logic circuit and said input and output signals of the first storage circuit.

8. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

a logical inversion circuit which serves to perform logical inversion of said carry signals;

an adder logic circuit which serves to sum up ~~the~~ an output signal of said logical inversion circuit and said output signals of the backward and forward coefficient multiplication circuits; and

a decoding circuit which serves to decode ~~the~~ an output signal of said adder logic circuit.

9. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

a logical inversion circuit which serves to perform logical inversion of said carry signals;

an adder logic circuit which serves to sum up ~~the~~ an output signal of said logical inversion circuit and said output signals of the backward and forward coefficient multiplication circuits; and

a decoding circuit which serves to decode ~~the~~ an output signal of said adder logic circuit and said input and output signals of the first storage circuit.

10. (currently amended) A digital filter ~~as claimed in claim 4~~ having a plurality of digital filter elements which are connected to each other in series, ~~wherein said~~ each digital filter element comprising:

a first adder logic circuit which receives a data input signal through a first input terminal;

a first shift register which is connected to said first adder logic circuit and receives ~~the~~ an output signal of said first adder logic circuit;

a clipping circuit which is connected to said first shift register and receives ~~the~~ an output signal of said first shift register;

a second shift register which is connected to said clipping circuit and receives ~~the~~ an output signal of said clipping circuit;

a third shift register which is connected to said second shift register and receives ~~the~~ an output signal of said second shift register;

a first coefficient multiplication circuit which is connected to said clipping circuit and receives ~~the~~ an output signal of said clipping circuit;

a second coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a third coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a fourth coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a fifth coefficient multiplication circuit which is connected to said third shift register and receives ~~the~~ an output signal of said third shift register;

a second adder logic circuit which is connected to said first coefficient multiplication circuit, said second coefficient multiplication circuit and said first adder logic circuit, and receives ~~the~~ output signals of said first coefficient multiplication circuit and said second coefficient multiplication circuit and outputs the sum thereof to a second input terminal of said first adder logic circuit;

a third adder logic circuit which is connected to said fourth coefficient multiplication circuit and said fifth coefficient multiplication circuit, and receives ~~the~~ output signals of said fourth and fifth coefficient multiplication circuits;

a fourth adder logic circuit which is connected to said third coefficient multiplication circuit and said third adder logic circuit, and receives ~~the~~ output signals of said third coefficient multiplication circuit and said third adder logic circuit and outputs the sum thereof as an output signal through an output terminal of said fourth adder logic circuit; and

an overflow detecting circuit which is connected to said first and second coefficient multiplication circuits, said first and second adder logic circuits at the current stage and connected to said third, fourth and fifth coefficient multiplication circuits and said third and fourth adder logic circuits at the preceding stage, receives ~~the~~ output signals of said first and second coefficient multiplication circuits, ~~the~~ carry output signals of said first and second adder logic circuits at the current stage and receives ~~the~~ output signals of said third, fourth and fifth coefficient multiplication circuits and ~~the~~ carry output signals of said third and fourth adder logic circuits at the preceding stage;

wherein said clipping circuit clips the output signal of said first shift register to either a positive or negative predetermined fixed value and outputs the clipped value in accordance with the output signal of said overflow detecting circuit.

11. (currently amended) A digital filter ~~as claimed in claim 4 wherein said~~ having a plurality of digital filter elements which are connected to each other in series, each digital filter element comprising:

a first adder logic circuit which receives a data input signal through a first input terminal;

a first shift register which is connected to said first adder logic circuit and receives ~~the~~ an output signal of said first adder logic circuit;

a clipping circuit which is connected to said first shift register and receives ~~the~~ an output signal of said first shift register;

a second shift register which is connected to said clipping circuit and receives ~~the~~ an output signal of said clipping circuit;

a third shift register which is connected to said second shift register and receives ~~the~~ an output signal of said second shift register;

a first coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a second coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a third coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a fourth coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a fifth coefficient multiplication circuit which is connected to said third shift register and receives ~~the~~ an output signal of said third shift register;

a second adder logic circuit which is connected to said first coefficient multiplication circuit and said second coefficient multiplication circuit, and receives ~~the~~ output signals of said first coefficient multiplication circuit and said second coefficient multiplication circuit;

a third adder logic circuit which is connected to said fourth coefficient multiplication circuit and said fifth coefficient multiplication circuit, and receives ~~the~~ output signals of said fourth and fifth coefficient multiplication circuits;

a fourth adder logic circuit which is connected to said third coefficient multiplication circuit and said third adder logic circuit, and receives ~~the~~ output signals of said third coefficient multiplication circuit and said third adder logic circuit and outputs ~~the~~ a sum thereof as an output signal through an output terminal of said fourth adder logic circuit;

a fifth adder logic circuit which is connected to said first and second adder logic circuits, receives ~~the~~ an output signal of said second adder logic circuit and a control signal for rounding off and output the sum thereof to a second input terminal of said first adder logic circuit; and

an overflow detecting circuit which is connected to said first and second coefficient multiplication circuits, said first, second and fifth adder logic circuits at the current stage and connected to said third, fourth and fifth coefficient multiplication circuits and said third and fourth adder logic circuits at the preceding stage, receives the output signals of said first and

second coefficient multiplication circuits, ~~the~~ carry output signals of said first, second and fifth adder logic circuits at the current stage and receives the output signals of said third, fourth and fifth coefficient multiplication circuits and the carry output signals of said third and fourth adder logic circuits at the preceding stage;

wherein said clipping circuit clips ~~the~~ an output signal of said first shift register to either a positive or negative predetermined fixed value and outputs the clipped value in accordance with the output signal of said overflow detecting circuit.

12. (currently amended) A digital filter ~~as claimed in claim 5 wherein said~~ having a plurality of digital filter elements which are connected to each other in series, each digital filter element comprising:

a first adder logic circuit which receives a data input signal through a first input terminal;

a first shift register which is connected to said first adder logic circuit and receives ~~the~~ an output signal of said first adder logic circuit;

a clipping circuit which is connected to said first shift register and receives ~~the~~ an output signal of said first shift register;

a second shift register which is connected to said clipping circuit and receives ~~the~~ an output signal of said clipping circuit;

a third shift register which is connected to said second shift register and receives ~~the~~ an output signal of said second shift register;

a first coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a second coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a third coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a fourth coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a fifth coefficient multiplication circuit which is connected to said third shift register and receives ~~the~~ an output signal of said third shift register;

a second adder logic circuit which is connected to said first coefficient multiplication circuit, said second coefficient multiplication circuit and said first adder logic circuit, and receives ~~the~~ output signals of said first coefficient multiplication circuit and said second coefficient multiplication circuit and outputs ~~the~~ a sum thereof to a second input terminal of said first adder logic circuit;

a third adder logic circuit which is connected to said fourth coefficient multiplication circuit and said fifth coefficient multiplication circuit, and receives ~~the~~ an output signal of said fourth and fifth coefficient multiplication circuits;

a fourth adder logic circuit which is connected to said third coefficient multiplication circuit and said third adder logic circuit, and receives the output signals of said third coefficient multiplication circuit and said third adder logic circuit and outputs ~~the~~ a sum thereof as an output signal through an output terminal of said fourth adder logic circuit; and

an overflow detecting circuit which is connected to said first and second coefficient multiplication circuits, said first and second adder logic circuits and said first shift register at the current stage and connected to said third, fourth and fifth coefficient multiplication circuits and said third and fourth adder logic circuits at the preceding stage, receives the output signals of said first and second coefficient multiplication circuits, ~~the~~ carry output signals of said first and second adder logic circuits and ~~the~~ input and intermediate tap output signals of said first shift register at the current stage and receives the output signals of said third, fourth and fifth coefficient multiplication circuits, the carry output signals of said third and fourth adder logic circuits at the preceding stage;

wherein said clipping circuit clips ~~the~~ an output signal of said first shift register to either a positive or negative predetermined fixed value and outputs ~~the~~ a clipped value in accordance with the output signal of said overflow detecting circuit.

13. (currently amended) A digital filter ~~as claimed in claim 5 wherein said~~ having a plurality of digital filter elements which are connected to each other in series, each digital filter element comprising:

a first adder logic circuit which receives a data input signal through a first input terminal;

a first shift register which is connected to said first adder logic circuit and receives ~~the~~ an output signal of said first adder logic circuit;

a clipping circuit which is connected to said first shift register and receives ~~the~~ an output signal of said first shift register;

a second shift register which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a third shift register which is connected to said second shift register and receives ~~the~~ an output signal of said second shift register;

a first coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a second coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a third coefficient multiplication circuit which is connected to said clipping circuit and receives the output signal of said clipping circuit;

a fourth coefficient multiplication circuit which is connected to said second shift register and receives the output signal of said second shift register;

a fifth coefficient multiplication circuit which is connected to said third shift register and receives ~~the~~ an output signal of said third shift register;

a second adder logic circuit which is connected to said first coefficient multiplication circuit and said second coefficient multiplication circuit, and receives ~~the~~ output signals of said first coefficient multiplication circuit and said second coefficient multiplication circuit;

a third adder logic circuit which is connected to said fourth coefficient multiplication circuit and said fifth coefficient multiplication circuit;

a fourth adder logic circuit which is connected to said third coefficient multiplication circuit and said third adder logic circuit, and receives ~~the~~ output signals of said third coefficient multiplication circuit and said third adder logic circuit and outputs ~~the~~ a sum thereof as an output signal through an output terminal of said fourth adder logic circuit;

a fifth adder logic circuit which is connected to said first and second adder logic circuits, receives ~~the~~ an output signals of said second adder logic circuit and a control signal for rounding off and output ~~the~~ a sum thereof to a second input terminal of said first adder logic circuit; and

an overflow detecting circuit which is connected to said first and second coefficient multiplication circuits, said first, second and fifth adder logic circuits and said first shift register at the current stage and connected to said third, fourth and fifth coefficient multiplication circuits and said third and fourth adder logic circuits at the preceding stage, receives the output signals of said first and second coefficient multiplication circuits, ~~the~~ carry output signals of said first, second and fifth adder logic circuits and ~~the~~ input and intermediate tap output signals of said first shift register at the current stage and receives ~~the~~ output signals of said third, fourth and fifth coefficient multiplication circuits, ~~the~~ carry output signals of said third and fourth adder logic circuits at the preceding stage;

wherein said clipping circuit clips the output signal of said first shift register to either a positive or negative predetermined fixed value and outputs ~~the~~ a clipped value in accordance with the output signal of said overflow detecting circuit.

14. (currently amended) The digital filter as claimed in claim 4 wherein said clipping circuit ~~comprising~~ comprises:

a data input terminal;

a data output terminal;

first and second overflow detection signal input terminals through which are input the output signals of said overflow detecting circuit;

first and second control signal input terminals through which timing signals are input;

a first storage circuit which serves to store an output signal of said clipping circuit; and

a second storage circuit which serves to store an internal signal of said clipping circuit,

wherein, said clipping circuit serves to save an input signal given through said data input terminal in said first storage circuit when the overflow detection signals indicate no overflow ~~during~~ while the timing signal input to said first control terminal is activated, to save 1 in said first storage circuit when the overflow detection signals indicate a positive overflow ~~during~~ while the timing signal input to said first control terminal is activated, and to save 0 in said first storage circuit when the overflow detection signals indicate a negative overflow ~~during~~ while the timing signal input to said first control terminal is activated, and

wherein, said clipping circuit serves to save 0 in said second storage circuit when the overflow detection signals indicate no overflow ~~during~~ while the timing signal input to said first control terminal is activated, to save 1 in said second storage circuit when the overflow detection signals indicate a positive or negative overflow ~~during~~ while the timing signal input to said first control terminal is activated, and to perform logical inversion of the value as saved in said first storage circuit when 1 is stored in said second storage circuit ~~during~~ while the timing signal input to said second control terminal is activated.

15. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ to output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits;

a sixth full adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ output signals of said fourth full adder circuit and ~~the~~ sum output signal of said fifth full adder circuit;

a seventh full adder circuit which is connected to said fifth and sixth full adder circuits and receives ~~the~~ output signals of said sixth full adder circuit and ~~the~~ carry output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of the sum output signal (/Z0) of said fourth full adder circuit, the sum output signal (/Z1) of said sixth full adder circuit and the sum output signal (Z2) and the carry output signal (/Z3) of said seventh full adder circuit in accordance with the logic equation $u = /Z3 \wedge (Z2 \vee Z1 \vee Z0)$ and $v = Z3 \wedge (/Z2 \vee /Z1 \vee /Z0)$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

16. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a sum output signal of said third full adder circuit;

a fourth inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a carry output signal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives ~~the~~ sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives ~~the~~ carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter;

a sixth full adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ output signals of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a seventh full adder circuit which is connected to said fifth and sixth full adder circuits and receives ~~the~~ a carry output signal of said fifth full adder circuit and ~~the~~ output signals of said sixth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of the sum output signal (/Z0) of said fourth full adder circuit, the sum output signal (/Z1) of said sixth full adder circuit and the sum output signal (Z2) and the carry output signal (/Z3) of said seventh full adder circuit in accordance with the logic equation $u = /Z3 \wedge (Z2 \vee Z1 \vee Z0)$ and $v = Z3 \wedge (/Z2 \vee /Z1 \vee /Z0)$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

17. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fourth inverters having input terminals connected respectively to said first through fourth carry signal input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and ~~the~~ to output terminals of said first through fourth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit;

a subtraction circuit which serves to subtract, from the numerical value 4 (binary expression: 0100), the numerical value represented by a binary number consisting of ~~the~~ a sum output signal (S0') of said fourth full adder circuit as a 0th bit, ~~the~~ a sum output signal (S1') of said first half adder circuit as a 1st bit, ~~the~~ a sum output signal (S2') of said second half adder

circuit as a 2nd bit and ~~the~~ a carry output signal (S3') of said second half adder circuit as a 3rd bit to generate the subtraction result of 4 bits (Z3, Z2, Z1 and Z0); and

a decoder which serves to generate overflow detection signals u and v by the use of the output signal of said subtraction circuit in accordance with the logic equation u = /Z3∧(Z2∨Z1∨Z0) and v = Z3∧(/Z2∨/Z1∨/Z0) and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

18. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

a first inverter having an input terminal connected to said fourth carry signal input terminal;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

second and third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and to ~~the~~ an output terminal of said first inverter;

a second inverter having an input terminal connected to said first full adder circuit and receives ~~the~~ a sum output signal of said first full adder circuit;

a third inverter having an input terminal connected to said first full adder circuit and receives ~~the~~ a carry output signal of said first full adder circuit;

a fourth full adder circuit which is connected to said second and third full adder circuits and said second inverter and receives ~~the~~ a sum output signals of said second and third full adder circuits and ~~the~~ an output signal of said second inverter;

a fifth full adder circuit which is connected to said second and third full adder circuits and said third inverter and receives ~~the~~ a carry output signal of said second and third full adder circuits and ~~the~~ an output signal of said third inverter;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit;

a subtraction circuit which serves to subtract, from the numerical value 4 (binary expression: 0100), the numerical value represented by a binary number consisting of ~~the~~ a sum output signal (S0') of said fourth full adder circuit as a 0th bit, ~~the~~ a sum output signal (S1') of said first half adder circuit as a 1st bit, ~~the~~ a sum output signal (S2') of said second half adder circuit as a 2nd bit and ~~the~~ a carry output signal (S3') of said second half adder circuit as a 3rd bit to generate the subtraction result of 4 bits (Z3, Z2, Z1 and Z0); and

a decoder which serves to generate overflow detection signals u and v by the use of the output signal of said subtraction circuit in accordance with the logic equation u = /Z3∧(Z2∨Z1∨Z0) and v = Z3∧ (/Z2∨/Z1∨/Z0)and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

19. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ an output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ a sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ a carry output signals of said first through third full adder circuits;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S1) of said first half adder circuit and ~~the~~ a sum output signal (S2) and the carry output signal (S3) of said second half adder circuit in accordance with the logic equation u = S3∨(S2∧S1) and v = /S3∧/S2 and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

20. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ an output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a sum output signal of said third full adder circuit;

a fourth inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a carry output signal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives ~~the~~ a sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives ~~the~~ a carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S1) of said first half adder circuit and the sum output signal (S2) and ~~the~~ a carry output signal (S3) of said second half adder circuit in accordance with the logic equation u = $S3 \vee (S2 \wedge S1)$ and v = $/S3 \wedge /S2$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

21. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fourth inverters having input terminals connected respectively to said first through fourth carry signal input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and ~~the~~ an output terminals of said first through fourth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ a sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ a carry output signals of said first through third full adder circuits;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S1') of said first half adder circuit and ~~the~~ a sum output signal (S2') and ~~the~~ a carry output signal (S3') of said second half adder circuit in accordance with the logic equation $u = /S3' \wedge /S2'$ and $v = S3' \vee (S2' \wedge S1')$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

22. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

a first inverter having an input terminal connected to said fourth carry signal input terminal;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

second and third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and to ~~the~~ an output terminal of said first inverter;

a second inverter having an input terminal connected to said first full adder circuit and receives ~~the~~ a sum output signal of said first full adder circuit;

a third inverter having an input terminal connected to said first full adder circuit and receives ~~the~~ a carry output signal of said first full adder circuit;

a fourth full adder circuit which is connected to said second and third full adder circuits and said second inverter and receives ~~the~~ a sum output signals of said second and third full adder circuits and ~~the~~ an output signal of said second inverter;

a fifth full adder circuit which is connected to said second and third full adder circuits and said third inverter and receives ~~the~~ a carry signals of said second and third full adder circuits and ~~the~~ an output signal of said third inverter;

a first half adder circuit which is connected to said fourth and fifth full adder circuits and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a second half adder circuit which is connected to said first half adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said first half adder circuit and ~~the~~ a carry output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S1') of said first half adder circuit and ~~the~~ a sum output signal (S2') and ~~the~~ a

carry output signal (S3') of said second half adder circuit in accordance with the logic equation u = /S3'∧/S2' and v = S3'∨(S2'∧S1') and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

23. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A) of said fourth full adder circuit and ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2) of said fifth full adder circuit in accordance with the logic equation u = P2∧(P1B∨P1A) and v = /P2∧ (/P1B∨/P1A) and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

24. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a sum output signal of said third full adder circuit;

a fourth inverter having an input terminal connected to said third full adder circuit and receives ~~the~~ a carry output signal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives ~~the~~ a sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives the carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A) of said fourth full adder circuit and ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2) of said fifth full adder circuit in accordance with the logic equation $u = P2 \wedge (P1B \vee P1A)$ and $v = /P2 \wedge (/P1B \vee /P1A)$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

25. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fourth inverters having input terminals connected respectively to said first through fourth carry signal input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and ~~the~~ output terminals of said first through fourth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A') of said fourth full adder circuit and ~~the~~ a sum output signal (P1B') and ~~the~~ a carry output signal (P2') of said fifth full adder circuit in accordance with the logic equation $u = /P2' \wedge (/P1B' \vee /P1A')$ and $v = P2' \wedge (P1B' \vee P1A')$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

26. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

a first inverter having an input terminal connected to said fourth carry input terminal;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

second and third full adder circuits having input terminals connected respectively to said first through fifth sign input terminals and to ~~the~~ an output terminal of said first inverter;

a second inverter having an input terminal connected to ~~the~~ a sum output terminal of said first full adder circuit;

a third inverter having an input terminal connected to ~~the~~ a carry output terminal of said first full adder circuit;

a fourth full adder circuit which is connected to said second and third full adder circuits and said second inverter and receives ~~the~~ sum output signals of said second and third full adder circuits and ~~the~~ an output signal of said second inverter;

a fifth full adder circuit which is connected to said second and third full adder circuits and said third inverter and receives ~~the~~ carry output signals of said second and third full adder circuits and ~~the~~ an output signal of said third inverter; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A') of said fourth full adder circuit and ~~the~~ a sum output signal (P1B') and ~~the~~ a carry output signal (P2') of said fifth full adder circuit in accordance with the logic equation $u = /P2' \wedge (/P1B' \vee /P1A')$ and $v = P2' \wedge (P1B' \vee P1A')$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

27. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second carry signal input terminals;

first through third sign input terminals;

first and second overflow detection signal output terminals;

first through third inverters having input terminals connected respectively to said first through third sign input terminals;

a first full adder circuit;

a half adder circuit, and said half adder circuit and said first full adder circuit have input terminals connected respectively to said first and second carry signal input terminals and ~~the~~ output terminals of said first through third inverters;

an AND gate which is connected to said half adder circuit and said first full adder circuit and receives ~~the~~ a sum output signal of said half adder circuit and ~~the~~ a sum output signal of said first full adder circuit;

a second full adder circuit which is connected to said AND gate, said half adder circuit and said first full adder circuit, receives ~~the~~ an output signal of said AND gate, ~~the~~ a carry output signal of said half adder circuit and ~~the~~ a carry output signal of said first full adder circuit and serves to output a carry output signal to said first overflow detection signal output terminal; and

a NOR gate which is connected to said second full adder circuit, receives ~~the~~ a sum output signal and the carry output signal of said second full adder circuit and serves to output a signal through said second overflow detection signal output terminal.

28. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second carry signal input terminals;

first through third sign input terminals;

first and second overflow detection signal output terminals;

a half adder circuit having input terminals connected respectively to said first and second carry signal input terminals;

a first full adder circuit having input terminals connected respectively to said first through third sign input terminals;

a first inverter having an input terminal connected to ~~the~~ a sum output terminal of said first full adder circuit;

a second inverter having an input terminal connected to ~~the~~ a carry output terminal of said first full adder circuit;

an AND gate having input terminals connected to ~~the~~ a sum output signal of said half adder circuit and ~~the~~ an output signal of said first inverter;

a second full adder circuit which is connected to said AND gate, said half adder circuit and said second inverter, receives ~~the~~ an output signal of said AND gate, ~~the~~ a carry output signal of said half adder circuit and ~~the~~ an output signal of said second inverter and outputs a carry output signal to said first overflow detection signal output terminal; and

a NOR gate which is connected to said second full adder circuit, receives ~~the~~ a sum output signal and the carry output signal of said second full adder circuit and serves to output a signal through said second overflow detection signal output terminal.

29. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second carry signal input terminals;

first through third sign input terminals;

first and second overflow detection signal output terminals;

first and second inverters having input terminals connected respectively to said first and second carry signal input terminals;

a first full adder circuit;

a half adder circuit, and said half adder circuit and said first full adder circuit have input terminals connected respectively to said first and second inverters and said first through third sign input terminals and receives ~~the~~ an output signal of said first and second inverters and ~~the~~ sign input signals through said first through third sign input terminals;

an AND gate which is connected to said half adder circuit and said first full adder circuit and receives ~~the~~ a sum output signal of said half adder circuit and ~~the~~ a sum output signal of said first full adder circuit;

a second full adder circuit which is connected to said AND gate, said half adder circuit and said first full adder circuit, receives ~~the~~ an output signal of said AND gate, ~~the~~ a carry output signal of said half adder circuit and ~~the~~ a carry output signal of said first full adder circuit and serves to output a carry output signal to said second overflow detection signal output terminal; and

a NOR gate which is connected to said second full adder circuit, receives ~~the~~ a sum output signal and ~~the~~ a carry output signal of said second full adder circuit and serves to output a signal through said first overflow detection signal output terminal.

30. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

first through fourth inverters having input terminals connected respectively to said first through fourth sign input terminals;

first and second full adder circuits having input terminals connected respectively to six terminals selected among from said first through third carry signal input terminals and ~~the~~ output terminals of said first through fourth inverters;

a third full adder circuit having input terminals connected respectively to the sum output terminals of said first and second full adder circuits and ~~the~~ an output terminal of said first through third carry signal input terminals and first through fourth inverters that is not connected to said first or second full adder circuits;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S0) of said third full adder circuit and ~~the~~ a sum output signal (S1) and ~~the~~ a carry output signal (S2) of said fourth full adder circuit in accordance with the logic equation u = S2∧(S1∨S0) and v = /S2∧(/S1∨/S0) and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

31. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

a first inverter having an input terminal connected to said first sign input terminal;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

a second full adder circuit having input terminals connected respectively to said second through fourth sign input terminals;

a second inverter having an input terminal connected to ~~the~~ a sum output terminal of said second full adder circuit;

a third inverter having an input terminal connected to ~~the~~ a carry output terminal of said second full adder circuit;

a third full adder circuit which is connected to said first full adder circuit and said first and second inverters and receives ~~the~~ a sum output signal of said first full adder circuit and ~~the~~ output signals of said first and second inverters;

a fourth full adder circuit which is connected to said third inverter and said first and third full adder circuits and receives ~~the~~ an output signal of said third inverter and the carry output signals of said first and third full adder circuits; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S0) of said third full adder circuit and ~~the~~ a sum output signal (S1) and ~~the~~ a carry output signal (S2) of said fourth full adder circuit in accordance with the logic equation u = S2∧(S1∨S0) and v = /S2∧(/S1∨/S0) and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

32. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

first through third inverters having input terminals connected respectively to said first through third carry signal input terminals;

first and second full adder circuits having input terminals connected respectively to six terminals selected among from said first through fourth sign input terminals and ~~the~~ output terminals of said first through third inverters;

a third full adder circuit having input terminals connected respectively to ~~the~~ sum output terminals of said first and second full adder circuits and the terminal that is one of said first through fourth sign input terminals and the output terminals of said first through third inverters and that is not connected to said first or second full adder circuits;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S0') of said third full adder circuit and ~~the~~ a sum output signal (S1') and ~~the~~ a carry output signal (S2') of said fourth full adder circuit in accordance with the logic equation u = /S2'∧(/S1'∨/S0') and v = S2'∧(S1'∨S0') and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

33. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

a first full adder ~~circuits~~ circuit having input terminals connected respectively to said first through third carry signal input terminals;

a second full adder circuit having input terminals connected respectively to said second through fourth sign input terminals;

a first inverter having an input terminal connected to ~~the~~ a sum output terminal of said first full adder circuit;

a second inverter having an input terminal connected to ~~the~~ a carry output terminal of said first full adder circuit;

a third full adder circuit which is connected respectively to said second full adder circuit, said first sign input terminal and said first inverter and receives ~~the~~ a sum output signal of said second full adder circuit, ~~the~~ a sign input signal through said first sign input terminal and ~~the~~ a output signal of said first inverter;

a fourth full adder circuit which is connected to said second and third full adder circuits and said second inverter and receives ~~the~~ carry output signals of said second and third full adder circuits and ~~the~~ an output signal of said second inverter; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a sum output signal (S0') of said third full adder circuit and ~~the~~ a sum output signal (S1') and ~~the~~ a carry output signal (S2') of said fourth full adder circuit in accordance with the logic equation u = /S2'∧(/S1'∨/S0') and v = S2'∧(S1'∨S0') and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

34. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fifth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said second through fifth carry signal input terminals and ~~the~~ output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits;

an AND gate having input terminals which ~~is~~ are connected respectively to said first carry signal input terminal and said fourth full adder circuit and receives ~~the~~ a carry input signal through said first carry signal input terminal and ~~the~~ a sum output signal of said fourth full adder circuit;

a half adder circuit which is connected respectively to said fourth full adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a output signal (P1A) of said AND gate, ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2A) of said half adder circuit and ~~the~~ a carry output signal (P2B) of said fifth full adder circuit in accordance with the logic equation $u = (P2B \wedge P2A) \vee [(P2B \vee P2A) \wedge (P1B \vee P1A)]$ and $v = /P2B \wedge /P2A \wedge (/P1B \vee /P1A)$ and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

35. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fifth carry signal input terminals;

first through fifth sign input terminals;

first and second overflow detection signal output terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said second through fifth carry signal input terminals and ~~the~~ output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to ~~the~~ a sum output terminal of said third full adder circuit;

a fourth inverter having an input terminal connected to ~~the~~ a carry output terminal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives ~~the~~ sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives ~~the~~ carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter;

an AND gate having input terminals which is connected respectively to said first carry signal input terminal and said fourth full adder circuit and receives ~~the~~ a carry input signal through said first carry signal input terminal and ~~the~~ a sum output signal of said fourth full adder circuit;

a half adder circuit which is connected respectively to said fourth full adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of the output signal (P1A) of said AND gate, the sum output signal (P1B) and the carry output signal (P2A) of said half adder circuit and the carry output signal (P2B) of said fifth full adder circuit in accordance with the logic equation u = (P2B∧P2A)∨[(P2B∨P2A) ∧(P1B∨P1A)] and v = /P2B∧/P2A∧(/P1B∨/P1A) and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

36. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through third sign input terminals;

first and second overflow detection signal output terminals;

first through third inverters having input terminals connected respectively to said first through third sign input terminals;

first and second full adder circuits having input terminals connected respectively to said first through third carry signal input terminals and ~~the~~ output terminals of said first through third inverters;

an AND gate which is connected to said first and second full adder circuits and receives ~~the~~ sum output signals ~~of said~~ of said first and second full adder circuits;

a third full adder circuit which is connected to said AND gate and said first and second full adder circuits, receives ~~the~~ an output signal of said AND gate and the carry output signals of said first and second full adder circuits and serves to output a carry output signal to said first overflow detection signal output terminal; and

a NOR gate which is connected to said third full adder circuit, receives ~~the~~ a sum output signal and ~~the~~ a carry output signal of said third full adder circuit and serves to output a signal through said second overflow detection signal output terminal.

37. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through third carry signal input terminals;

first through third sign input terminals;

first and second overflow detection signal output terminals;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

a second full adder circuit having input terminals connected respectively to said first through third sign input terminals;

a first inverter having an input terminal connected to ~~the~~ a sum output terminal of said second full adder circuit;

a second inverter having an input terminal connected to ~~the~~ a carry output terminal of said second full adder circuit;

an AND gate having input terminals connected to said first full adder circuit and said first inverter and receives ~~the~~ a sum output signal of said first full adder circuit and ~~the~~ an output signal of said first inverter;

a third full adder circuit which is connected to said AND gate, said first full adder circuit and said second inverter, receives ~~the~~ an output signal of said AND gate, ~~the~~ a carry output signal of said first full adder circuit and ~~the~~ an output signal of said second inverter and outputs a carry output signal to said first overflow detection signal output terminal; and

a NOR gate which is connected to said third full adder circuit, receives ~~the~~ a sum output signal and ~~the~~ a carry output signal of said third full adder circuit and serves to output a signal through said second overflow detection signal output terminal.

38. (currently amended) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

first through fourth inverters having input terminals connected respectively to said first through fourth carry signal input terminals;

first and second full adder circuits;

a half adder circuit, and said half adder circuit and said first and second full adder circuits have input terminals connected respectively to said first through fourth sign input terminals and ~~the~~ output terminals of said first through fourth inverters;

a third full adder circuit which is connected to said first and second full adder circuits and said half adder circuit and receives ~~the~~ sum output signals of said first and second full adder circuits and ~~the~~ a sum output signal of said half adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said half adder circuit and receives ~~the~~ carry output signals of said first and second full adder circuits and ~~the~~ a carry output signal of said half adder circuit; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A') of said third full adder circuit and ~~the~~ a sum output signal (P1B') and ~~the~~ a carry output signal (P2') of said fourth full adder circuit in accordance with the logic equation u = /P2'∧(/P1B'∨/P1A') and v = P2'∧(P1B'∨P1A') and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

39. (currently added) The digital filter as claimed in claim 4 wherein said overflow detecting circuit ~~comprising~~ comprises:

first through fourth carry signal input terminals;

first through fourth sign input terminals;

first and second overflow detection signal output terminals;

a first inverter having an input terminal connected to said fourth carry signal input terminal;

a first full adder circuit having input terminals connected respectively to said first through third carry signal input terminals;

a second full adder circuit;

a half adder circuit, and said half adder circuit and said second full adder circuit have input terminals connected respectively to ~~the~~ an output terminal of said first inverter and said first through fourth sign input terminals;

a second inverter having an input terminal connected to ~~the~~ a sum output terminal of said first full adder circuit;

a third inverter having an input terminal connected to ~~the~~ a carry output terminal of said first full adder circuit;

a third full adder circuit which is connected to said second inverter, said second full adder circuit and said half adder circuit and receives ~~the~~ an output signal of said second inverter, ~~the~~ a sum output signal of said second full adder circuit and ~~the~~ a sum output signal of said half adder circuit;

a fourth full adder circuit which is connected to said half adder circuit, said second full adder circuit and said third inverter and receives ~~the~~ a carry output signal of said half adder circuit, ~~the~~ a carry output signal of said second full adder circuit and ~~the~~ an output signal of said third inverter; and

a decoder which serves to generate overflow detection signals u and v by the use of ~~the~~ a carry output signal (P1A') of said third full adder circuit and ~~the~~ a sum output signal (P1B') and ~~the~~ a carry output signal (P2') of said fourth full adder circuit in accordance with the logic equation u = /P2'∧(/P1B'∨/P1A') and v = P2'∧(P1B'∨P1A') and output the overflow detection signals u and v respectively through said first and second overflow detection signal output terminals.

40. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

a plurality of carry signal input terminals;

a plurality of sign input terminals;

first and second data bit input terminals through which first and second data bits (k,l) are received; and

first and second overflow detection signal output terminals,

wherein said overflow detecting circuit serves to generate internal overflow detection signals with reference to said plurality of ~~the~~ carry signal input terminals and said plurality of ~~the~~ sign input terminals and when overflow is detected, to output said internal overflow detection signals, and when overflow is not detected, to output, as overflow detection signals, signals indicative of a positive overflow in the case where said first data bit (k) is 0 and said second data bit (l) is 1 and signals indicative of a negative overflow in the case where said first data bit (k) is 1 and said second data bit (l) is 0.

41. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second data bit input terminals through which first and second data bits are received;

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits;

a decoder which serves to generate first and second output signals u and v by the use of ~~the~~ a carry output signal (P1A) of said fourth full adder circuit and ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2) of said fifth full adder circuit in accordance with the logic equation $u = P2 \wedge (P1B \vee P1A)$ and $v = /P2 \wedge (/P1B \vee /P1A)$;

a sixth inverter having an input terminal connected to said first data bit input terminal;

a seventh inverter having an input terminal connected to said second data bit input terminal;

an eighth inverter which is connected to said decoder and receives ~~the~~ a first output signal of said decoder;

a ninth inverter which is connected to said decoder and receives ~~the~~ a second output signal of said decoder;

a first AND gate which is connected to said sixth inverter, said second data bit input terminal and said ninth inverter and receives ~~the~~ an output signal of said sixth inverter, ~~the~~ an

input signal through said second data bit input terminal and the output signal of said ninth inverter;

a second AND gate which is connected to said seventh inverter, said first data bit input terminal and said eighth inverter and receives ~~the~~ an output signal of said seventh inverter, ~~the~~ an input signal through said first data bit input terminal and ~~the~~ an output signal of said eighth inverter;

a first OR gate which is connected to said first AND gate and said decoder, receives ~~the~~ an output signal of said first AND gate and ~~the~~ a first output signal of said decoder and outputs a positive overflow detection signal; and

a second OR gate which is connected to said second AND gate and said decoder, receives ~~the~~ an output signal of said second AND gate and ~~the~~ a second output signal of said decoder and outputs a negative overflow detection signal.

42. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second data bit input terminals through which first and second data bits are received;

first through fourth carry signal input terminals;

first through fifth sign input terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said first through fourth carry signal input terminals and ~~the~~ output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to ~~the~~ a sum output terminal of said third full adder circuit;

a fourth inverter having an input terminal connected to ~~the~~ a carry output terminal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives the sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives ~~the~~ carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter;

a decoder which serves to generate first and second output signals u and v by the use of ~~the~~ a carry output signal (P1A) of said fourth full adder circuit and ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2) of said fifth full adder circuit in accordance with the logic equation $u = P2 \wedge (P1B \vee P1A)$ and $v = /P2 \wedge (/P1B \vee /P1A)$;

a fifth inverter having an input terminal connected to said first data bit input terminal;

a sixth inverter having an input terminal connected to said second data bit input terminal;

a seventh inverter which is connected to said decoder and receives ~~the~~ a first output signal of said decoder;

an eighth inverter which is connected to said decoder and receives ~~the~~ a second output signal of said decoder;

a first AND gate which is connected to said fifth inverter, said second data bit input terminal and said eighth inverter and receives ~~the~~ an output signal of said fifth inverter, ~~the~~ an input signal through said second data bit input terminal and ~~the~~ an output signal of said eighth inverter;

a second AND gate which is connected to said sixth inverter, said first data bit input terminal and said seventh inverter and receives ~~the~~ an output signal of said sixth inverter, ~~the~~ an input signal through said first data bit input terminal and ~~the~~ an output signal of said seventh inverter;

a first OR gate which is connected to said first AND gate and said decoder, receives ~~the~~ an output signal of said first AND gate and ~~the~~ a first output signal of said decoder and output a positive overflow detection signal; and

a second OR gate which is connected to said second AND gate and said decoder, receives ~~the~~ an output signal of said second AND gate and ~~the~~ a second output signal of said decoder and output a negative overflow detection signal.

43. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second data bit input terminals through which first and second data bits are received;

first through fifth carry signal input terminals;

first through fifth sign input terminals;

first through fifth inverters having input terminals connected respectively to said first through fifth sign input terminals;

first through third full adder circuits having input terminals connected respectively to said second through fifth carry signal input terminals and ~~the~~ output terminals of said first through fifth inverters;

a fourth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ sum output signals of said first through third full adder circuits;

a fifth full adder circuit which is connected to said first through third full adder circuits and receives ~~the~~ carry output signals of said first through third full adder circuits;

a first AND gate having input terminals which is connected respectively to said first carry signal input terminal and said fourth full adder circuit and receives ~~the~~ a carry input signal through said first carry signal input terminal and ~~the~~ a sum output signal of said fourth full adder circuit;

a half adder circuit which is connected respectively to said fourth full adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a decoder which serves to generate first and second output signals u and v by the use of ~~the~~ an output signal (P1A) of said first AND gate, ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2A) of said half adder circuit and ~~the~~ a carry output signal (P2B) of said fifth full adder circuit in accordance with the logic equation $u = (P2B \wedge P2A) \vee [(P2B \vee P2A) \wedge (P1B \vee P1A)]$ and $v = /P2B \wedge /P2A \wedge (/P1B \vee /P1A)$;

a sixth inverter having an input terminal connected to said first data bit input terminal;

a seventh inverter having an input terminal connected to said second data bit input terminal;

an eighth inverter which is connected to said decoder and receives ~~the~~ a first output signal of said decoder;

a ninth inverter which is connected to said decoder and receives ~~the~~ a second output signal of said decoder;

a second AND gate which is connected to said sixth inverter, said second data bit input terminal and said ninth inverter and receives ~~the~~ an output signal of said sixth inverter, the input signal through said second data bit input terminal and ~~the~~ an output signal of said ninth inverter;

a third AND gate which is connected to said seventh inverter, said first data bit input terminal and said eighth inverter and receives ~~the~~ an output signal of said seventh inverter, the input signal through said first data bit input terminal and ~~the~~ an output signal of said eighth inverter;

a first OR gate which is connected to said second AND gate and said decoder, receives ~~the~~ an output signal of said second AND gate and ~~the~~ a first output signal of said decoder and outputs a positive overflow detection signal; and

a second OR gate which is connected to said third AND gate and said decoder, receives ~~the~~ an output signal of said third AND gate and ~~the~~ a second output signal of said decoder and outputs a negative overflow detection signal.

44. (currently amended) The digital filter as claimed in claim 5 wherein said overflow detecting circuit ~~comprising~~ comprises:

first and second data bit input terminals through which first and second data bits are received;

first through fifth carry signal input terminals;

first through fifth sign input terminals;

first and second inverters having input terminals connected respectively to said first and second sign input terminals;

first and second full adder circuits having input terminals connected respectively to said second through fifth carry signal input terminals and ~~the~~ output terminals of said first and second inverters;

a third full adder circuit having input terminals connected respectively to said third through fifth sign input terminals;

a third inverter having an input terminal connected to ~~the~~ a sum output terminal of said third full adder circuit;

a fourth inverter having an input terminal connected to ~~the~~ a carry output terminal of said third full adder circuit;

a fourth full adder circuit which is connected to said first and second full adder circuits and said third inverter and receives ~~the~~ a sum output signals of said first and second full adder circuits and ~~the~~ an output signal of said third inverter;

a fifth full adder circuit which is connected to said first and second full adder circuits and said fourth inverter and receives ~~the~~ a carry output signals of said first and second full adder circuits and ~~the~~ an output signal of said fourth inverter;

a first AND gate having input terminals which is connected respectively to said first carry signal input terminal and said fourth full adder circuit and receives ~~the~~ a carry input signal through said first carry signal input terminal and ~~the~~ a sum output signal of said fourth full adder circuit;

a half adder circuit which is connected respectively to said fourth full adder circuit and said fifth full adder circuit and receives ~~the~~ a carry output signal of said fourth full adder circuit and ~~the~~ a sum output signal of said fifth full adder circuit;

a decoder which serves to generate first and second output signals u and v by the use of ~~the~~ an output signal (P1A) of said first AND gate, ~~the~~ a sum output signal (P1B) and ~~the~~ a carry output signal (P2A) of said half adder circuit and ~~the~~ a carry output signal (P2B) of said fifth full adder circuit in accordance with the logic equation $u = (P2B \wedge P2A) \vee [(P2B \vee P2A) \wedge (P1B \vee P1A)]$ and $v = /P2B \wedge /P2A \wedge (/P1B \vee /P1A)$;

a fifth inverter having an input terminal connected to said first data bit input terminal;

a sixth inverter having an input terminal connected to said second data bit input terminal;

an seventh inverter which is connected to said decoder and receives ~~the~~ a first output signal of said decoder;

a eighth inverter which is connected to said decoder and receives ~~the~~ a second output signal of said decoder;

a second AND gate which is connected to said fifth inverter, said second data bit input terminal and said eighth inverter and receives ~~the~~ an output signal of said fifth inverter, the input signal through said second data bit input terminal and ~~the~~ an output signal of said eighth inverter;

a third AND gate which is connected to said sixth inverter, said first data bit input terminal and said seventh inverter and receives ~~the~~ an output signal of said sixth inverter, the input signal through said first data bit input terminal and ~~the~~ an output signal of said seventh inverter;

a first OR gate which is connected to said second AND gate and said decoder, receives ~~the~~ an output signal of said second AND gate and ~~the~~ a first output signal of said decoder and outputs a positive overflow detection signal; and

a second OR gate which is connected to said third AND gate and said decoder, receives ~~the~~ an output signal of said third AND gate and ~~the~~ a second output signal of said decoder and outputs a negative overflow detection signal.

45. (currently amended) The digital filter as claimed in claim 5 wherein said clipping circuit ~~comprising~~ comprises:

a data input terminal;

a data output terminal;

first and second overflow detection signal input terminals through which are input the output signals of said overflow detecting circuit;

first and second control signal input terminals through which timing signals are input;

a first storage circuit which serves to store an output signal of said clipping circuit; and

a second storage circuit which serves to store an internal signal of said clipping circuit,

wherein, said clipping circuit serves to save an input signal given through said data input terminal in said first storage circuit when the overflow detection signals indicate no overflow ~~during~~ while the timing signal input to said first control terminal is activated, to save 1 in said first storage circuit when the overflow detection signals indicate a positive overflow ~~during~~ while the timing signal input to said first control terminal is activated, and to save 0 in said first storage circuit when the overflow detection signals indicate a negative overflow ~~during~~ while the timing signal input to said first control terminal is activated, and

wherein, said clipping circuit serves to save 0 in said second storage circuit when the overflow detection signals indicate no overflow ~~during~~ while the timing signal input to said first control terminal is activated, to save 1 in said second storage circuit when the overflow detection signals indicate a positive or negative overflow ~~during~~ while the timing signal input to said first control terminal is activated, and to perform logical inversion of the value as saved in said first

storage circuit when 1 is stored in said second storage circuit ~~during~~ while the timing signal input to said second control terminal is activated.